WHAT IS CLAIMED IS:

1. A phase change memory cell array, comprising:

a plurality of word lines;

a plurality of bit lines intersecting the word lines;

a plurality of memory cells arranged in rows along the word lines and located at corresponding intersection regions of the word lines and bit lines, respectively, wherein each of the memory cells includes (a) a cell transistor having a gate connected to a corresponding word line, and (b) a resistor and a phase change cell connected in series between a drain of the cell transistor and a corresponding bit line; and

a plurality of auxiliary transistors respectively connected between the drains of the cell transistors of adjacent said memory cells.

2. The phase change memory array of claim 1, wherein a gate of each of the auxiliary transistors is connected to a same word line as a gate of at least one of the respective cell transistors of the adjacent memory cells.

3. The phase change memory array of claim 1, wherein a gate of each of the auxiliary transistors is connected to a same word line as the gates of the respective cell transistors of the adjacent memory cells.

4. The phase change memory array of claim 1, further comprising a plurality of dummy cell transistor pairs connected at opposite ends of the word lines, respectively.

5. The phase change memory array of claim 1, wherein the cell transistors are MOS transistors.

6. The phase change memory array of claim 1, wherein the cell transistors are bipolar junction transistors.

7. A phase change memory array, comprising:

a plurality of word lines;

a plurality of bit lines intersecting the word lines;

a plurality of memory cells arranged in rows along the word lines and located at corresponding intersection regions of the word lines and bit lines, respectively, wherein each of the memory cells includes (a) a cell transistor having a gate connected to a corresponding word line, and (b) a resistor and a phase change cell connected in series between a drain of the cell transistor and a corresponding bit line; and

a plurality of vertical gates respectively interposed between the drains of the cell transistors of adjacent said memory cells, wherein each of the vertical gates extends from and in a same layer as a corresponding word line.

8. The phase change memory array of claim 7, wherein each vertical gate is connected to a same word line as the gates of the respective cell transistors of the adjacent memory cells.

9. The phase change memory array of claim 7, further comprising a plurality of dummy cell transistor pairs, each of which is located at both ends of each of the word lines.

10. The phase change memory array of claim 7, wherein the cell transistors are MOS transistors.

11. The phase change memory array of claim 7, wherein the cell transistors are bipolar junction transistors.

12. A phase change memory array, comprising:

a plurality of word line pairs;

a plurality of bit lines intersecting the word line pairs;

a plurality of memory cells arranged in rows between the word lines of a corresponding word line pair and located at intersection regions of the word line pairs and bit lines, respectively, wherein each of the memory cells includes (a) a cell transistor having a gate connected to a corresponding word line pair, and (b) a resistor and a phase change cell connected in series between a drain of the cell transistor and

a corresponding bit line; and

a plurality of vertical gates respectively interposed between the drains of the cell transistors of adjacent said memory cells, wherein each of the vertical gates is connected between the word lines of a corresponding word line pair and in a same layer as the corresponding word line pair.

13. The phase change memory array of claim 12, wherein each vertical gate is connected to a same word line as the gates of the respective cell transistors of the adjacent memory cells.

14. The phase change memory array of claim 12 further comprising a plurality of dummy cell transistor pairs, each of which is located at both ends of each of the word line pairs.

15. The phase change memory array of claim 12, wherein one word line of each word line pair is interposed between row memory array blocks.

16. The phase change memory array of claim 12, wherein each word line pair is interposed between row memory array blocks.

17. The phase change memory array of claim 12, wherein a region of the array of memory cells is devoid of a shallow trench isolation (STI) structure.

18. The phase change memory array of claim 12, wherein each vertical gate extends obliquely between the word lines of the corresponding word line pair.

19. The phase change memory array of claim 12, wherein the cell transistors are MOS transistors.

20. The phase change memory array of claim 12, wherein the cell transistors are bipolar junction transistors.

21. A phase change memory array,

comprising:

a plurality of word line pairs;

a plurality of bit lines intersecting the word line pairs;

a plurality of memory cells arranged in rows between the word lines of a corresponding word line pair and located at intersection regions of the word line pairs and bit lines, respectively, wherein each of the memory cells includes (a) a cell transistor having a gate connected to a corresponding word line pair, and (b) a resistor and a phase change cell connected in series between a drain of the cell transistor and a corresponding bit line; and

a plurality of vertical gates respectively connected at one end between the word lines of a respective word line pair and in a same layer as the respective word line pair.

22. The phase change memory array of claim 21 further comprising a plurality of dummy cell transistor pairs, each of which is located at both ends of each of the word lines.

23. The phase change memory array of claim 21, wherein one word line of each word line pair is interposed between row memory array blocks.

24. The phase change memory array of claim 21, wherein each word line pair is interposed between row memory array blocks.

25. The phase change memory array of claim 21, wherein columns of the phase change cells are separated by shallow trench isolation (STI).

26. The phase change memory array of claim 21, wherein the cell transistors are MOS transistors.

27. The phase change memory array of claim 21, wherein the cell transistors are bipolar junction transistors.